Course Name	**ECE 55801 Advanced Systems on a Chip (SoC) Designs for Image Processing using FPGAs**
Credit and contact hours	(3 cr.) Class 3
Course coordinator's name	Lauren Christopher
Textbook	By: Crockett H Louise, Northcote David), Ramsay Craig Exploring Zynq MPSoC: With PYNQ and Machine Learning Applications, ISBN-13: 978-0992978761, ISBN-10 0992978769
Course Information	**2020-21 IUPUI Campus Bulletin description:** **ECE 55801 Advanced Systems on a Chip (SoC) Designs for Image Processing using FPGAs (3 cr.)** P: ECE 42100 and ECE 30100 or consent of instructor or Graduate standing. Class 3. This class covers advanced concepts in using Field Programmable Gate Arrays (FPGAs) designed with an HDL (VHDL for example: Very High Speed IC Hardware Description Language). The students will learn complex interface design, advanced hardware and embedded system design and parallel processing. Projects and lessons will focus on applications in Digital Imaging Systems. Lecture and projects covering topics including: VHDL mapped to FPGA for state machine design, hardware and software VGA control, image filtering, data transfer to bus, and embedded controller integration. Graduate standing or consent of instructor. **Prerequisites/ CoRequisite** P: ECE 421 and ECE 301; or Graduate Standing
Goals for the course	Upon successful completion of the course, students should be able to 1. Design and simulate complex systems for FPGA using a Hardware Description Language [1,6] 2. Map system designs to FPGA hardware [1,2,6] 3. Develop FPGA system with embedded software [1,2,6] 4. Apply FPGA design to image processing problems [1,2,6] 5. Team-develop a novel design of an imaging system on the FPGA and present to class. [1,2,3,5,6]
List of topics to be covered	1. Course Instructions, introduction and review (2 classes) 2. System Design with VHDL (3 classes) 3. Extended and Advanced Design with FPGAs (3 classes) 4. Image Processing with FPGA (4 classes) 5. Student Final Team Project (4 classes) 6. Quizzes and Exams (2-4 classes) Laboratory Projects: The course will include homework and Xilinx board lab design projects. This will involve programming in VHDL or Verilog and the use of simulation tools and hands-on experiments with FPGA development boards. The students will submit short

	project reports for the individual small projects. Final Project will be a team effort which requires the students to submit a written project report and give a presentation.
Syllabi Approved by	Lauren Christopher
Date of Approval	04/09/2019