Course name	**ECE 27000 Digital Logic Design**
Credit and contact hours	(4 cr.) Class 3, Lab 1
Course coordinator's name	Lauren Christopher
Textbook	Charles H. Roth, Jr. and Larry L. Kinney, *Fundamentals of Logic Design,* 7th Ed., 2014, Cengage, ISBN 1133628478
Course information	**2020-21 IUPUI Campus Bulletin description:** ECE 27000 Digital Logic Design (4 cr.) P: or C: ECE 20100 and knowledge of electrical circuits. Class 3, Lab 3. Introduction to logic design, with emphasis on practical design techniques and circuit implementation. Topics include Boolean algebra; theory of logic functions; mapping techniques and function minimization; hardware description language; logic equivalent circuits and symbol transformations; electrical characteristics; propagation delays; signed number notations and arithmetic; binary and decimal arithmetic logic circuits; theory of sequential circuits; timing diagrams; analysis and synthesis of SR-, D-, T-, and JK-based sequential circuits; clock generation circuits; algorithmic state machine method of designing sequential circuits. A series of logic circuit experiments using CMOS integrated circuits for combination of logic and sequential circuits. **Prerequisites/ Co-Requisite** P or C: ECE 20100 **Required, Elective, or Selected Elective:** EE Required, CE Required
Goals for the course	Upon successful completion of the course, students should be able to 1. Derive a Boolean expression for a digital circuit. [1, 6] 2. Design a digital circuit given the input, output and description of the system. [1, 2, 6] 3. Design sequential logic and combinational logic digital circuits. [6] 4. Design digital circuits using various digital logic building blocks such as multiplexers and Flip-Flops. [1, 2] 5. Derive a finite state machine, implement it and optimize it given a description of the target digital system. [1, 2, 6] 6. Reverse engineer a digital circuit. That is, given a digital circuit design, be able to determine functionality. [1, 6]
List of topics to be covered	1. Introduction: CMOS switches, numbers, binary arithmetic, ICs. (1 class) 2. Logic operations; truth tables; logic gates. (3 classes) 3. Boolean algebra and canonical forms. (2 classes)

	4. K-maps; minimization of logic functions. (3 classes) 5. Multilevel combinational logic. (1 class) 6. Multiplexers, demultiplexers. (1 class) 7. Time response and hazards. (1 class) 8. Programmable logic. (1 class) 9. Tri-state and open collector gates; combinational logic case study. (2 classes) 10. Latches and Flip-Flops (2 classes) 11. Finite state machines, implementation and optimization (4 classes) 12. Arithmetic Unit: Adders/subtractors/multipliers. (2 classes) 13. Exams/Quizzes. (3 classes) 14. Final exam. (final exam period) **Laboratory projects** 1. Logic Circuit 2. Boolean algebra 3. Multi-level Combinational Logic 4. MUX, Decoder and PLA/ROM 5. Multi-level Combinational Logic 6. Latch and Flip Flop 7. Programmable Logic Device 8. Finite State Machine 9. Final Design Project
Syllabi approved by	Lauren Christopher
Date of approval	04/09/2019