Elective Course:	**ECE 595 Advanced Systems on a Chip (SoC) Designs for Image Processing using FPGAs**
Credit and contact hours:	(3 cr.) Class 3
2012-14 IUPUI Campus Bulletin description:	ECE 595 Advanced Systems on a Chip (SOC) Designs for Image Processing using FPGAs. Credit 3. This class covers advanced concepts in using Field Programmable Gate Arrays (FPGAs) designed with an HDL (VHDL for example: Very High Speed IC Hardware Description Language). The students will learn complex interface design, advanced hardware and embedded system design and parallel processing. Projects and lessons will focus on applications in Digital Imaging Systems. Lecture and projects covering topics including: VHDL mapped to FPGA for state machine design, hardware and software VGA control, image filtering, data transfer to PCI bus, and embedded controller integration.
Prerequisite or corequisite:	P ECE 421 and ECE 301; or Graduate Standing
Prerequisites by topic:	Advanced Digital System Design using VHDL and FPGA, Discrete Time Fourier Transform, Discrete Fourier Transform.
Textbooks:	Pedroni, Volnei A., *Circuit Design and Simulation with VHDL,* 2nd Edition, MIT Press, ISBN-10: 0262014335 | ISBN-13: 978-0262014335 Various papers and projects.
Coordinator:	Lauren Christopher, Assistant Professor of Electrical and Computer Engineering
Goals:	To introduce FPGA design for image processing to advanced undergraduate and beginning graduate students. Students will learn 2D and 3D imaging techniques through projects designed on the FPGA hardware.
Outcomes:	Upon successful completion of the course, students should be able to 1. Design and simulate complex systems for FPGA using and HDL [a, b, c] 2. Map system designs to FPGA hardware [a, b, c, e, k] 3. Develop FPGA system with embedded software [a, b, c, e, k] 4. Apply FPGA design to image processing problems [a, b, c, e] 5. Use a team to develop a novel design of an imaging system on the FPGA [c, d, k]
Topics:	1. Course Instructions, introduction and review (2 classes) 2. System Design with VHDL (3 classes) 3. Extended and Advanced Design with FPGAs (3 classes) 4. Image Processing with FPGA (4 classes) 5. Student Final Team Project (4 classes) 6. Quizzes and Exams (2-4 classes)
Computer usage:	The students are required to use Mentor Graphics Modelsim and Xilinx ISE software. They need to write their own Verilog/VHDL code for design projects.
Evaluation methods:	One midterm exam, homework, laboratory reports, final project report, and final comprehensive exam.
Laboratory projects:	The course will include homework and Xilinx board lab design projects. This will involve programming in VHDL or Verilog and

	the use of simulation tools and hands-on experiments with FPGA development boards. The students will submit short project reports for the individual small projects. Final Project will be a team effort which requires the students to submit a written project report and give a presentation.
Grading:	10% Textbook Homework 30% 3 Lab Projects 25% Final Project 10% Mid-Term Exam 25% Final Exam
ABET category:	Engineering science 50%, engineering design 50%.
Prepared by:	Lauren Christopher
Date:	May 9, 2012

Administrative Withdrawal: A basic requirement of this course is that you will participate in class and conscientiously complete writing and reading assignments. Keep in touch with me if you are unable to attend class or complete an assignment on time. If you miss more than half our class meetings within the first four weeks of the semester without contacting me, you will be administratively withdrawn from this section. Our class meets twice per week; thus if you miss more than four classes in the first four weeks, you may be withdrawn. Administrative withdrawal may have academic, financial, and financial aid implications. Administrative withdrawal will take place after the full refund period, and if you are administratively withdrawn from the course you will not be eligible for a tuition refund. If you have questions about the administrative withdrawal policy at any point during the semester, please contact me.

During the semester, if you find that life stressors are interfering with your academic or personal success, consider contacting IUPUI's Counseling and Psychological Services (CAPS). All IUPUI students are eligible for individual counseling services at minimal fees. Group counseling services are free of charge. CAPS also performs evaluations for learning disorders and ADHD; fees are charged for testing. CAPS is located in Walker Plaza, Room 220 (719 Indiana Avenue) and can be contacted by phone (317-274-2548). For more information, see the CAPS web-site at: http://life.iupui.edu/caps/.