Required Course:	**ECE 55900 MOS VLSI Design**
Credit and contact hours:	(3 cr.) Class 3
2014-16 IUPUI Campus Bulletin description:	ECE 55900 MOS VLSI Design (3 cr.) P: ECE 30500 and ECE 36500 or Graduate Standing. Class 3. Introduction to most aspects of large-scale MOS integrated circuit design, including device fabrication and modeling; useful circuit building blocks; system considerations; and algorithms to accomplish common tasks. Most circuits discussed are treated in detail, with particular attention given those whose regular and/or expandable structures are primary candidates for integration. All circuits are digital and are considered in the context of the silicon-gate MOS enhancement-depletion technology. Homework requires the use of existing IC mask layout software; term projects assigned.
Prerequisite or corequisite:	ECE 305 or consent of instructor
Prerequisites by topic:	*Semiconductor devices (pn-junction diodes, BJTs, MOSFETs), digital logic (Boolean functions, logic building blocks, finite state machines), computer organization (datapath, control, memory hierarchy, arithmetic algorithms).*
Textbook:	*Principles of CMOS VLSI Design: A Systems Perspective*, Third Edition, N.H.E. Weste and David Harris, Addison Wesley, ISBN 0-321-14901-7
Coordinator:	Lauren Christopher, Assistant Professor of Electrical and Computer Engineering
Goals:	
Outcomes:	*A student who successfully fulfills the course requirements will have demonstrated:* i. an ability to analyze MOS circuits. [a,b,c,d] ii. an ability to synthesize MOS circuits. [c,e,k] iii. experience in oral presentation, teamwork, and document preparation for a finished design. [b, c] iv. an ability to create and simulate a hierarchical digital design using commercial grade CAD software.. [b,c,e,k]
Topics:	**Lecture Outline:** 1-2: Introduction: Historical Perspective and Future Trends; CMOS Process

	2-4: MOS devices, SPICE models 5-7: Inverters 8-10: Designing combinational logic gates in CMOS 11-13: Designing sequential circuits 14-15 Interconnect and timing issues 16-17 Designing memory and array structures 18-20 Designing arithmetic building blocks 21-23 VLSI testing and verification 24-25: System design issues 26-27: Project Presentations Mid term exams take two lectures
Computer usage:	**Mentor Graphics** PSpice Circuit Simulation
Laboratory projects:	
Evaluation methods:	Five short exams (45 minute each), two PSpice design projects, 10 homework assignments, and a comprehensive final exam.
ABET category:	Engineering science 1.5 credit or 50%, Engineering design 1.5 credits or 50%
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