Required Course:	**ECE 42100 Advanced Digital System Design**
Credit and contact hours:	(3 cr.) Class 3
2014-16 IUPUI Campus Bulletin description:	ECE 42100 Advanced Digital System Design (3 cr.) P: ECE 27000 and ECE 26300. Class 3. Advanced topics in digital design. Boolean logic. Logic optimization, VLSI and ASIC design basics. Design. Simulation. Placement and routing. Logic synthesis. FPGA structure. FPGA implementation. FPGA design flow. Verilog and VHDL coding.
Prerequisite or corequisite:	P ECE 27000. ECE 26300
Prerequisites by topic:	Digital Logic, Computer programming.
Textbooks:	Ashenden, Peter, *Digital Design, an Embedded Systems Approach Using VHDL*, Elsevier, 2008, ISBN 978-0-12-369528-4. Agans, David J., *Debugging: the 9 indispensable rules for finding even the most elusive software and hardware problems*, AMACOM, 2002, ISBN: 0-8144-7457-8.
Coordinator:	Lauren Christopher, Assistant Professor of Electrical and Computer Engineering
Goals:	FPGA-based digital design using VHDL or Verilog is fundamental for many engineering applications. In this course, the students will study digital design, Verilog or VHDL, VLSI, and FPGA, and get exposure to the complete hardware design flow, Verilog/VHDL programming and hands-on experiences in FPGA design and debugging.
Outcomes:	Upon successful completion of the course, students should be able to 1. Understand complex digital design principles [b, e] 2. Write synthesizable Verilog/VHDL programs [c, k] 3. Understand FPGA structure and usage [b, e] 4. Understand ASIC and FPGA design flow [b, c, e] 5. Design, verify and test complex digital system in FPGA hardware [a, b, c, e]
Topics:	1. Course Instructions, advanced topics in logic (2 classes) 2. Advanced topics in sequential logic (3 classes) 3. VLSI design basics (3 classes) 4. FPGA structure (4 classes) 5. Verilog/VHDL basics (4 classes) 6. Advanced Verilog/VHDL coding (4 classes) 7. FPGA design flow based on Verilog/VHDL (4 classes) 8. FPGA system implementation, verification and testing (4 classes) 9. Quizzes and Exams (2-4 classes)
Computer usage:	The students are required to use Mentor Graphics Modelsim and Xilinx ISE software. They need to write their own Verilog/VHDL code for design projects.
Evaluation methods:	One or more midterm exams/quizzes, homework, laboratory reports, final project report, and final comprehensive exam.
Laboratory projects:	The course will include homework and Xilinx board lab design projects. This will involve programming in VHDL or Verilog and the use of simulation tools and hands-on experiments with FPGA development boards. The students will submit short project reports

	for the individual small projects. Final Project will be a team effort which requires the students to submit a written project report and give a 10-minute presentation. Design 1: VHDL for basic logic Design 2: VHDL for VGA hardware Design 3: Using VHDL with IP blocks Design 4: Integrating Embedded Processor, adding SW to HW Final Project: – Student selected
Grading:	15% for ~20 homework 20% for ~10 lab modules 25% for final project 20% for best 2 out of 3 quizzes 20% for comprehensive final
ABET category:	Engineering science 50%, engineering design 50%.
Prepared by:	Lauren Christopher
Date:	July 24, 2014

Administrative Withdrawal: A basic requirement of this course is that you will participate in class and conscientiously complete writing and reading assignments. Keep in touch with me if you are unable to attend class or complete an assignment on time. If you miss more than half our class meetings within the first four weeks of the semester without contacting me, you will be administratively withdrawn from this section. Our class meets twice per week; thus if you miss more than four classes in the first four weeks, you may be withdrawn. Administrative withdrawal may have academic, financial, and financial aid implications. Administrative withdrawal will take place after the full refund period, and if you are administratively withdrawn from the course you will not be eligible for a tuition refund. If you have questions about the administrative withdrawal policy at any point during the semester, please contact me.

During the semester, if you find that life stressors are interfering with your academic or personal success, consider contacting IUPUI's Counseling and Psychological Services (CAPS). All IUPUI students are eligible for individual counseling services at minimal fees. Group counseling services are free of charge. CAPS also performs evaluations for learning disorders and ADHD; fees are charged for testing. CAPS is located in Walker Plaza, Room 220 (719 Indiana Avenue) and can be contacted by phone (317-274-2548). For more information, see the CAPS web-site at: http://life.iupui.edu/caps/.